IN THE SPECIFICATION

Please amend the paragraph beginning on page 19, line 4 as follows:

FIG. 14 is a circuit diagram of an input inversion controller according to an embodiment of the invention. Input inversion controller 1400 may be used as [[output]] input inversion controller 312 of FIG. 3. In FIG. 14, data bits DI-0 through DI-N on lines 391 represent the input data bits DQ (0-N) in a write operation when data is inputted to memory device 100 (FIG. 1). For simplicity, DI-0 through DI-N are referred to as DI.

Please amend the paragraph beginning on page 19, line 15 as follows:

Input inversion controller 1400 includes a control unit 1410, an input data storage 1425, and an input inverting unit 1430. Input data storage 1425 stores a number of groups of data bits DI-0 through [[DO-N]] DI-N provided from lines [[392]] 391 during a write cycle. The number of groups of data bits DI-0 through DO-N have corresponding input inverting codes Ii-0 through Ii-M. Each input inverting code carries inversion information of a corresponding [[groups]] group of data bits. Ii-0 through Ii-M are provided to input inversion controller 1400 on auxiliary lines 1411, which connect to lines 391. For clarity, FIG. 14 does not show the connections between lines 1411 and lines 391. Control unit 1410 enables input inverting unit 1430 whether or not to invert the each group of data bits stored in input data storage 1425 based on the Ii-0 through Ii-M codes. Input inverting unit 1430 provides either the inverted or the true version of the groups of data bits DI-0 through DI-N to input data path 111.